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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,595	09/09/2003	Paul Elliott	851963.413	1920

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EXAMINER	
PATEL, NIMESH G	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 03/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/658,595	ELLIOTT, PAUL	
	Examiner	Art Unit	
	Nimesh G. Patel	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20040301*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cavanna et al.(US 6,208,703), in view of Holm et al.(US 6,687,255).

3. Regarding claim 1, Cavanna discloses a bridge circuit for use in retiming in a semiconductor integrated circuit, the bridge circuit comprising: an initiator interface(Figure 2, Write Interface); a target interface(Figure 2, Read Interface); a storage buffer circuit having a data input connected to the initiator interface and a data output connected to the target interface, and having a plurality of storage locations; and a storage buffer control circuit associated with the storage buffer circuit; the storage buffer control circuit comprising: a write pointer register(Figure 2, 41) connected to the storage buffer circuit and clocked at the storage buffer input clock rate(Figure 2, 57) to control the storage location at which data is written into the storage buffer circuit; a read pointer register(Figure 2, 51) connected to the storage buffer circuit and clocked at the storage buffer output clock rate(Figure 2, 49) to control the storage location from which data is read from the storage buffer circuit; a first retiming circuit(Figure 2, 63, 42) coupled to the output of the read pointer register to retime the output of the read pointer register with reference to the storage buffer input clock rate(Figure 2, 57); a second retiming circuit(Figure 2, 46, 64) coupled to the output of the write pointer register to retime the output of the write pointer register with reference to the storage buffer output clock rate(Figure 2, 49); a first comparator(Figure 2, 44) connected to receive and compare the outputs of the write pointer

register and the first retiming circuit and to provide an output(Figure 2, 56) dependent thereon; a second comparator(Figure 2, 47) connected to receive and compare the outputs of the read pointer register and the second retiming circuit and to provide an output(Figure 2, 48) dependent thereon; write control logic(Figure 2, 45) connected to receive the output of the first comparator and connected to the write pointer register to increment the count held in the write pointer register in dependence upon the output of the first comparator; and read control logic(Figure 2, 50) connected to receive the output of the second comparator and connected to the read pointer register to increment the count held in the read pointer register in dependence upon the output of the second comparator; and wherein the write control logic in the storage buffer control circuit is adapted to control the write pointer register such that data received at the data input of the associated storage buffer circuit is written into successive storage locations of the storage buffer circuit as the data is received so long as the storage locations are not all full(Figure 2, 56), and the read control logic in the storage buffer control circuit is adapted to control the read pointer register such that data in the storage locations are read from successively and the contents applied to the data output of the storage buffer circuit.

Cavanna does not specifically disclose that the storage locations are not read until a predetermined time delay. However, Holm discloses storage locations being read after a predetermined time delay(Column 2, Lines 4-7 and 50-55). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teachings of Cavanna and Holm to wait to read the storage locations after a predetermined delay since this is typically done in FIFOs and to increase tolerance for delays that may be occasioned by latency and overhead(Column 2, Lines 9-13).

4. Regarding claim 2, Holm discloses a bridge circuit wherein the predetermined time delay is a predetermined number of clock cycles of either buffer input or output clock(Column 2, Lines 50-55).

5. Regarding claim 3, Holm discloses a bridge circuit, wherein the predetermined time delay is when a predetermined number of storage locations are full(Column 2, Lines 4-7).

6. Regarding claim 4, Holm discloses a bridge circuit, in which the read control logic also causes all the full storage locations to be read from on receipt of an end-of-packet signal(Column 3, Lines 1-10).

7. Regarding claim 5, Cavanna discloses a bridge circuit, in which the comparators provide outputs indicating at least when the storage buffer circuit is full and is empty(Figure 2, 26, 28).

8. Regarding claim 6, Cavanna discloses a bridge circuit, in which the maximum number of storage locations to be made available simultaneously is predetermined, the write control logic is adapted to determine when the storage buffer circuit is full(Figure 2, 26).

9. Regarding claim 7, Holm discloses a bridge circuit, in which each retiming circuit includes a Gray coder clocked at the input clock rate of the retiming circuit.(Column 8, Lines 48-50).

10. Regarding claim 8, Cavanna discloses a bridge circuit, in which each retiming circuit is adapted to provide a plurality of possible degrees of retiming, and including a mode signal input for receiving a mode signal indicating the currently required degree of retiming, the retiming circuit being responsive to the mode signal to provide the required degree of retiming(Figures 7 and 8).

11. Regarding claim 9, Cavanna discloses a bridge circuit, in which each retiming circuit includes two retiming elements connected in cascade, and a selector, the selector being connected to receive the input to the retiming elements and the output of each of the retiming

elements and to select one of its inputs as the output in dependence upon the mode signal(Figure 2, Items 63, 42, 46, 64).

12. Regarding claim 10, Cavanna discloses a bridge circuit, in which the mode signal is adapted to be changed during operation of the bridge circuit(Figures 7 and 8).

13. Regarding claim 11, Cavanna discloses a bridge circuit, further comprising a strobe retiming circuit connected to receive a strobe signal and retime it relative to the initiator clock, an edge detector for detecting an edge in the strobe signal, a mode signal timing circuit for timing the mode signal relative to the output of the edge detector, and a mode signal change detection circuit connected to the output of the mode signal timing circuit to detect a change in the mode signal and to provide a change signal in response thereto(Column 8, Lines 27-46).

14. Regarding claim 12, Cavanna discloses a bridge circuit, further comprising a bypass for the storage buffer circuit, and a selector for selecting either the storage buffer circuit or the bypass in accordance with a mode signal received at an input(Column 8, Lines 27-46).

15. Regarding claim 13, Holm discloses a bridge circuit, further comprising a second storage buffer circuit having a data input connected to the target interface and a data output connected to the initiator interface and a data output connected to the initiator interface and having a plurality of storage locations, and a second storage buffer control circuit similar to the first-mentioned storage buffer control circuit connected to control the second storage buffer circuit(Figure 2, 16, 18).

16. Regarding claim 14, Holm discloses a semiconductor integrated circuit comprising at least one bridge circuit in accordance with claim 1(Figure 1).

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

17. Claims 15-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Cavanna.

18. Regarding claim 15, Cavanna discloses a bridge circuit for use in retiming in a semiconductor integrated circuit, the bridge circuit comprising: an initiator interface(Figure 2, Write Interface); a target interface(Figure 2, Read Interface); a storage buffer circuit having a data input connected to the initiator interface and a data output connected to the target interface, and having a plurality of storage locations; and a storage buffer control circuit associated with the storage buffer circuit; the storage buffer control circuit comprising: a write pointer register(Figure 2, 41) connected to the storage buffer circuit and clocked at the storage buffer input clock rate(Figure 2, 57) to control the storage location at which data is written into the storage buffer circuit; a read pointer register(Figure 2, 51) connected to the storage buffer circuit and clocked at the storage buffer output clock rate(Figure 2, 49) to control the storage location from which data is read from the storage buffer circuit; a first retiming circuit(Figure 2, 63, 42) coupled to the output of the read pointer register to retime the output of the read pointer register with reference to the storage buffer input clock rate(Figure 2, 57) comprising one or more retiming buffers(Figure 2, 63, 42) and a selector connected to receive inputs from each of the retiming buffers; a second retiming circuit(Figure 2, 46, 64) coupled to the output of the write pointer register to retime the output of the write pointer register with reference to the storage buffer output clock rate(Figure 2, 49) comprising one or more retiming buffers(Figure 2, 63, 42) and a selector connected to receive inputs from each of the retiming buffers; a first comparator(Figure 2, 44) connected to receive and compare the outputs of the write pointer register and the first retiming circuit and to provide an output(Figure 2, 56) dependent thereon; a second comparator(Figure 2, 47) connected to receive and compare the outputs of the read pointer register and the second retiming circuit and to provide an output(Figure 2, 48) dependent thereon; write control logic(Figure 2, 45) connected to receive the output of the first

comparator and connected to the write pointer register to increment the count held in the write pointer register in dependence upon the output of the first comparator; and read control logic(Figure 2, 50) connected to receive the output of the second comparator and connected to the read pointer register to increment the count held in the read pointer register in dependence upon the output of the second comparator; and wherein the write control logic in the storage buffer control circuit is adapted to control the selectors such that zero or more retiming buffers are selectively in the path from the read or write pointer registers to the comparators(Column 8, Lines 27-46).

19. Regarding claim 16, Cavanna discloses a bridge circuit, in which each retiming circuit is adapted to provide a plurality of possible degrees of retiming, and including a mode signal input for receiving a mode signal indicating the currently required degree of retiming, the retiming circuit being responsive to the mode signal to provide the required degree of retiming(Figures 7 and 8).

20. Regarding claim 17, Cavanna discloses a bridge circuit, in which each retiming circuit includes two retiming elements connected in cascade, and a selector, the selector being connected to receive the input to the retiming elements and the output of each of the retiming elements and to select one of its inputs as the output in dependence upon the mode signal(Figure 2, Items 63, 42, 46, 64).

21. Regarding claim 18, Cavanna discloses a bridge circuit, in which the mode signal is adapted to be changed during operation of the bridge circuit(Figures 7 and 8).

22. Regarding claim 19, Cavanna discloses a bridge circuit, wherein each retiming buffer comprises a D-type flip-flop for each bit in the pointer register output, whereby zero or more D-type flip-flops are selectively chosen for retiming(Figure 2, Items 63, 42, 46, 64).

23. Regarding claim 20, Cavanna discloses a bridge circuit, wherein selectively 0, 1 or 2 D-type flip-flops are selected for retiming(Column 8, Lines 27-46).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nimesh G. Patel whose telephone number is 571-272-3640. The examiner can normally be reached on M-F, 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nimesh G Patel
Examiner
Art Unit 2112

NP
March 14, 2006

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
3/16/06